**ECE -1 Lab **

**Experiment - 8**

**Aim:** Sequential system design using state Machines

Description:

Part1:

1. Write a VHDL code of mod 4 up/down counter using state machines. The counter has a Reset signal to reset the current count to 0, another control signal count to decide the up or down count. If count =0, then it acts like up counter and as a down counter for count =1.Output of the counter is current state of the machine. Show at least 20 clock cycles in your testbench.
2. A sequential system has 0,1,2,3 inputs (Code them in binary for coding purpose). The system has an output Z which is 1 if the system has odd numbers of 1’s and even number of 2’s in the whole sequence at a given time, else the output is 0. Write a VHDL code for the system using state machines. Show at least 25 clock cycles in your testbench and output should be 1 at least 4 times in that sequence.
3. Write a VHDL code for a sequential system using state machine which recognizes the pattern 1101 in a sequence of 0’s and 1’s. The system has a input x and output z. z is 1 if x(t-3,t) = 1101, else 0. Show at least 4 detections of pattern 1101 in your testbench.

Part2:

1. For each type of the above implementations generate the synthesis report.
2. Study delay, power and cell usage for each implementation.
3. Generate the corresponding testbench to verify the design.